CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate having a first portion for an MRAM and a second portion for a first circuit type, wherein the first circuit type is different than MRAM;

first front end circuitry for the MRAM over the first portion in the substrate;

second front end circuitry for the first circuit type in the second portion of the substrate;

an MRAM cell over the first front end circuitry, wherein the MRAM cell uses a first metal layer for a first program line; and

a metal interconnect over the second front end circuitry, wherein the metal interconnect uses the first metal layer to provide interconnect for the first circuit type.

2. The semiconductor device of claim 1, wherein the MRAM cell is further characterized as using a second metal layer for a second program line and the metal interconnect is further characterized as using the second metal layer to provide interconnect for the first type of circuitry.

3. The semiconductor device of claim 2, further comprising a third metal layer over the first and second metal layers and a fourth metal layer over the third metal layer, wherein the third and fourth metal layers are both thicker than the first and second metal layers.

4. The semiconductor device of claim 3, wherein the third and fourth metal layers have substantially the same thickness.

5. The semiconductor device of claim 4 wherein a portion of the first metal layer functions as a digit line.

6. The semiconductor device of claim 5, wherein a portion of the second metal line functions as a bit line.

7. The semiconductor device of claim 4, wherein the third and fourth layers are separated by a first distance and the second and third layers are separated by a second distance, wherein the second distance is greater than the first distance.

8. The semiconductor device of claim 4, wherein the third and fourth layers are separated by a first distance and the second and third layers are separated by a second distance, wherein the second distance is substantially equal to the first distance.

9. The semiconductor device of claim 3, wherein the fourth layer is thicker than the third layer.

10. The semiconductor device of claim 9, wherein the third and fourth metal layers are connected by vias of a first width and the third and second metal layers are connected by vias of a second width greater than the first width.

11. The semiconductor device of claim 1, further comprising:

a third metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, wherein the first portion of the third metal layer is immediately over the second metal layer and the second portion of the third metal layer is immediately over the third metal layer.

12. The semiconductor device of claim 1, wherein the MRAM uses the second metal layer for a second program line.

13. The semiconductor device of claim 1, further comprising a third metal over the second metal layer, wherein the third metal layer has a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, wherein the second portion is substantially coterminous with the second layer and is connected to the second layer by a plurality of vias.

14. The semiconductor device of claim 13, wherein the MRAM cell uses the second metal layer for a second program line.

15. A semiconductor device, comprising:

a semiconductor substrate having a first portion for an MRAM and a second portion for a circuit of a type different than MRAM; and

a first metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, wherein the first portion of the first metal layer is used as a first program line for the MRAM and the second portion of the first metal line is used for interconnecting the circuit.

16. The semiconductor device of claim 15, a second metal layer over the first metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, wherein the first portion of the second metal layer is used for a second program line of the MRAM and the second portion of the second metal layer is used for interconnecting the circuit.

17. The semiconductor device of claim 16, further comprising a third metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, wherein

the second portion of the third metal layer is connected to the second portion of the second layer by a first via having a first length;

the second portion of the second metal layer is connected to the second portion of the first metal layer by a second via having a second length greater than the first length.

18. The semiconductor device of claim 17, wherein the third metal layer is the last metal layer of the semiconductor device.

19. The semiconductor device of claim 17, wherein the second portions of the second and third metal layers are substantially conterminous.

20. The semiconductor device of claim 17, further comprising a fourth metal layer over the third metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate.

21. The semiconductor device of claim 20, wherein the fourth metal layer has a thickness greater than that of the third metal layer.

22. The semiconductor device of claim 20, wherein the fourth metal layer is connected to the third metal layer by a

23. The semiconductor device of claim 15, further comprising a second metal layer over the first metal layer over the first portion of the substrate used for a second program line of the MRAM.

24. The semiconductor device of claim 23, further comprising a third metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, wherein the first portion of the third metal layer is immediately over the second metal layer and the second portion of the third metal layer is immediately over the first metal layer.

25. The semiconductor device of claim 24, further comprising:

a first via connecting the first portion of the second metal layer to the first portion of the first metal layer, the first via having a first length; and

a second via connecting the second portion of the third metal layer to the second portion of the first metal layer, the second via having a second length greater than the first length.

26. A method of making a semiconductor device, comprising:

providing a semiconductor substrate;

forming a MRAM circuitry on and in a first portion of the substrate;

forming first circuitry of a type different than MRAM in and on a second portion of the substrate;

forming a first metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, the second portion of the first metal layer for interconnecting the first circuit;

forming a portion of an MRAM cell over the first portion of the first metal layer using the first portion of the first metal layer as a first program line of the MRAM cell.

27. The method of claim 26, further comprising forming a second metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, the second portion of the second metal layer for interconnecting the first circuit and the first portion of the second metal layer for providing a second program line of the MRAM cell.

28. The method of claim 26, further comprising

forming a second metal layer over the first metal line for providing a second program line of the MRAM cell; and

forming a third metal layer having a first portion over the first portion of the substrate and a second portion over the second portion of the substrate, the second portion of the third metal layer being immediately over the first metal layer for interconnecting the first circuit and the first portion of the third metal layer being immediately over the second metal layer.